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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,004	04/01/2004	Darius D. Gaskins	CNTR.2216	9571

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EXAMINER	
PATEL, ANAND B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,004	GASKINS, DARIUS D.	
	Examiner	Art Unit	
	Anand Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-11,15-18 and 20* is/are rejected.

7)☒ Claim(s) *5-8,12-14 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: paragraph 2 does not contain the serial number of the copending application.

Appropriate correction is required.

Double Patenting

2. Claims 1-4, 10-11, 15-18, 20 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4, 8, 11-12, 14, 17-20 of copending Application No. 10/816020 in view of US Patent No 6836849 to Brock et al (Brock).

- Claim 1 claims the same invention as claim 1 of the copending application except voltage control logic that adjusts voltage commensurate with frequency. Brock teaches adjusting voltage according to changes in frequency. Motivation to modify the instant application with the voltage adjusting as taught by Brock is the ability to optimize costs and performance.
- Claim 2 in view of Brock claims the same invention as claim 4 of the copending application.
- Claim 3 in view of Brock claims the same invention as claim 2 of the copending application.
- Claim 4 in view of Brock claims the same invention as claim 3 of the copending application.
- Claim 10 in view of Brock claims the same invention as claim 8 of the copending application.
- Claim 11 in view of Brock claims the same invention as claims 11, 12 of the copending application.
- Claim 15 in view of Brock claims the same invention as claim 14 of the copending application.
- Claim 16 in view of Brock claims the same invention as claim 17 of the copending application.
- Claim 17 in view of Brock claims the same invention as claim 18 of the copending application.
- Claim 18 in view of Brock claims the same invention as claim 19 of the copending application.

- Claim 20 in view of Brock claims the same invention as claim 20 of the copending application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 9, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No 6259293 to Hayase et al (Hayase) in view of Applicant's Admitted Prior Art (AAPA) and Brock.

- As per claim 1, Hayase discloses a frequency-voltage mechanism for power management, comprising:
  - A first PLL (top PLL, 9) that generates a first source clock signal at a first frequency based on a clock signal (figure 14);
  - A second PLL (middle PLL, 9) that generates a second source clock signal at a second frequency based on a clock signal (figure 14);
  - Select logic (10) that selects between said first and second source clock signals to provide a core clock signal based on a select signal (column 2, lines 13-20; inherent that 10 has a select signal input).

  Hayase fails to disclose clock control logic and voltage control logic. AAPA teaches:
  - A programmable PLL (105) that generates a clock signal at a programmable frequency (paragraphs 5-6) based on a frequency control signal (CORERATIO) and a bus clock signal (BUS CLOCK);

- Clock control logic (103) that detects power conditions via at least one power sense signal (101), that provides said first frequency control signal according to said power conditions (figure 1).

An advantage of the system taught by AAPA is the ability to lower power in the system (paragraph 6). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Hayase with the clock control logic as taught by AAPA. Motivation to modify is to cut power costs.

AAPA fails to disclose voltage control logic. Brock teaches voltage control logic that adjusts operating voltage commensurate with frequency of said core clock signal (column 3, lines 57-67). An advantage of the system taught by Brock is the ability to optimize performance (column 2, lines 23-31). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Hayase and AAPA with the voltage control logic as taught by Brock. Motivation to modify is to lower costs and increase performance.

- As per claim 9, Brock teaches wherein said clock control logic and said voltage control logic cooperate to increase said operating voltage prior to increasing frequency of said core clock signal and to decrease said operating voltage after decreasing frequency of said core clock signal (column 3, lines 57-67).
- As per claim 15, Hayase discloses a frequency-voltage control for microprocessor power management, comprising:
  - Generating a first source clock at a first frequency based on a clock (figure 14);
  - Generating a second source clock at a second frequency based on a clock and an input (figure 14);
  - Switching between the first and second source clock signals (column 2, lines 13-20).

AAPA teaches:

- Sensing power conditions (101); and
- A PLL generating a clock based on a bus clock signal and a ratio bus value (paragraph 6; figure 1).

Brock teaches selecting operating voltage commensurate with the core operating frequency (column 3, lines 57-67).

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayase in view of AAPA, Brock and US Patent No 6448834 to Takaki.

- As per claim 2, Hayase, AAPA, and Brock fail to disclose switching clocks within one clock cycle. Takaki teaches switching clocks within one clock cycle (column 3, lines 16-19). An advantage of the system taught by Takaki is the ability to remove clock drift when changing clocks (column 1, lines 26-44). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Hayase, AAPA, and Brock with the clock switching time limit as taught by Takaki. Motivation to modify is to improve system reliability and decrease clock drift errors.

6. Claims 3, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayase in view of AAPA, Brock and US Patent No 7019577 to Agrawal et al (Agrawal).

- As per claim 3, Hayase and AAPA fail to disclose a lock signal. Agrawal teaches wherein the PLL generates a lock signal when said clock signal is at a frequency indicated by said frequency control signal (column 4, lines 45-46). An advantage of the system taught by Agrawal is the ability to improve clock generation techniques (column 1, lines 23-31). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Hayase and AAPA with the clock signal as taught by Agrawal. Motivation to modify is to cut costs and wasted time.
- As per claim 10, Hayase discloses a microprocessor, comprising:
  - A first PLL (top PLL, 9) that provides said first core clock signal at a first frequency based on a signal (figure 14);

- A second PLL (middle PLL, 9) that generates a second core source clock signal at a frequency based on a signal (figure 14);
- Select logic (10) that selects between said first and second PLLs based on said select signal to provide a core clock signal (column 2, lines 13-20; inherent that 10 has a select signal input).

AAPA teaches:

- A power condition sense interface (interface receiving 101) receiving at least one power sense signal indicative of power conditions (101);
- A clock controller (103), coupled to said power condition sense interface (figure 1), that provides a core ratio bus value to control frequency of said first source signal (paragraph 6);
- A programmable PLL (105), coupled to said clock source controller (figure 1), that generates a clock signal at a programmable frequency (paragraphs 5-6) based on a frequency control signal (CORERATIO) and a bus clock signal (BUS CLOCK).

Brock teaches an operating voltage interface (inherent given voltage used to drive the system) and a voltage controller that adjusts operating voltage commensurate with frequency of said core clock signal (column 3, lines 57-67).

Agrawal teaches a PLL that outputs a lock signal indicating that said core clock frequency is operative (column 4, lines 45-46).

Allowable Subject Matter

7. Claims 4-8, 11-14, 16-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and amended or disclaimed to overcome the double patenting rejection above. Prior art fails to disclose or suggest wherein said clock control logic controls said select signal to switch said core clock signal from said first PLL to said second PLL in response to said first frequency lock signal.

Prior art also fails to disclose or suggest wherein said first PLL generates said first clock source signal based on a second frequency control signal and that asserts a second lock signal indicative thereof, and wherein said clock control logic provides said second frequency control signal and receives said second lock signal. Prior art fails to disclose or suggest the specific method of switching, including wherein: said second PLL generates said second source signal at a maximum power frequency level; wherein said clock controller initially selects said second PLL, determines a reduced power level sufficient to meet said power conditions, provides said first core ratio bus value indicative of a reduced frequency of said core clock signal to achieve said reduced power level, and switches said select signal to select said first PLL in response to receiving said first lock signal; wherein said first PLL ramps said first source signal to said reduced frequency and provides said first lock signal indicative thereof; and wherein said voltage controller reduces operating voltage commensurate with said reduced frequency after said clock controller switches said core clock signal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anand Patel whose telephone number is (571) 272-7211. The examiner can normally be reached on Mon-Fri 8AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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ABP